REMARKS

Drawing Objections

The Examiner has objected to Figures 1 and 2 as lacking the legend "Prior Art" since only that which is old is illustrated. Formal drawings (FIGS. 1-4) are submitted with this Amendment with FIGS. 1 and 2 showing the legend "Prior Art".

Specification Objections

The Examiner has objected to the disclosure because of informalities. Specifically, the Examiner indicates that on page 2, line 30 of the specification, the number "02" should read "102". A corrected specification paragraph correcting the incorrect number "02" to the correct number "102" is provided with this response.

Reply to 35 U.S.C. 112 Rejection

The Examiner has rejected claim 13 under 35 U.S.C. 112 because in lines 1-2 there is insufficient antecedent basis for the limitation "the one wire bus". Claim 13 has been amended to now depend on claim 8 which provides the requisite antecedent basis for the limitation "the one wire bus".

Reply to 35 U.S.C. 102 Rejections

The Examiner has rejected 1-4 and 7-11 under 35 U.S.C. 102(b) as being anticipated by Tsukahara (U.S.P. No. 5,592,108). In particular the Examiner asserts that Tsukahara discloses an interface circuit including an active pull-up device (4);

a level shift circuit (5) coupled to the active pull-up device (4) wherein the active pull-up device (4) is coupled to a one wire bus and the level shift circuit is also coupled to circuit ground (VSS) as recited in claim 1. The Examiner applies the same reasoning to claim 7 and similarly rejects claims 7-11.

Applicants respectfully disagree with the Examiner's characterization of Tsukahara and it's application to the claims 1-4 and 7-11 of the present invention. Tsukahara is directed to an interface circuit that includes an input current limiting circuit for limiting a current of an input signal fed from a preceding circuit, thereby outputting a current limiting signal to a following circuit. The interface circuit also includes a level shifting circuit for converting a level of the current-limited signal to a logic level of the following circuit.

In contrast thereto, the present invention provides a circuit for reducing the adverse effects of noise and capacitance in a one-wire bus to which a plurality of I-button devices are connected. As shown in Fig. 4, the circuit of the present invention comprises an active pull-up device (306) on a one wire bus coupled to a level shift circuit (304). The level shift circuit is connected to circuit ground and thus replaces ground as the reference level for the active pull up device. Claim 1 clearly recites that in the present invention a level shift circuit is coupled to an active pull-up device wherein the active pull up device is coupled to both a one wire bus and to circuit ground.

Contrary to the Examiner's assertions, Tsukahara does not disclose these limitations. As clearly shown in Fig. 1 of Tsukahara, the interface circuit disclosed therein shows a level pull-up circuit coupled to a level shifting circuit that is in turn coupled to a power supply voltage VSS (see Tsukahara column 2, line 66) and an output

stage circuit(6). Tsukahara simply does not disclose a level shift circuit on a one-wire bus connected to a pull-up circuit and circuit ground as disclosed by the present invention. Accordingly Tsukahara does not anticipate claims 1 or 7 of the present invention and these claims are allowable. Claims 2-4 and 8-11 are also allowable and not anticipated by Tsukahara, at least by virtue of their dependence on claims 1 and 7 respectively.

The Examiner has rejected claims 1-3, 5-10 and 12-13 under U.S.C. 102(b) as being anticipated by Turner et al (U.S.P. No. 6,118,302). In particular the Examiner asserts that Turner discloses in Fig. 13 an interface for low voltage semiconductor devices comprising an active pull up device (1330) ; a level-shift circuit (1317) coupled to the active pull-up device (1330) wherein the active pull-up device (1330) is coupled to a one wire bus (1310) and the level-shift circuit (1317) is also coupled to circuit ground (1341) as recited in claim 1. Applicants respectfully disagree with the Examiner's characterization of Turner and respectfully traverse this rejection as follows.

Contrary to the Examiner's assertion Turner does not disclose a level shift circuit (1317) coupled to an active pull up device (1330) coupled to a one wire bus (1310). In fact the Examiner mischaracterizes the elements in Turner. Firstly, element 1330 is not an active pull-up device but rather a voltage down converter (see Turner column 20 line 14) and secondly element 1310 is not a one wire bus asserted by the Examiner but rather refers to the core of a chip (see Turner, column 20 lines 14-15). Accordingly, the Examiner's characterization of Turner is flawed and Turner simply does not disclose the elements and limitations recited in independent claims 1 and 7 of the present invention. Accordingly Turner does not anticipate claims 1 and 7 of the present invention and these

claims are allowable. Dependent claims 2-3, 5, 8-10 and 12-13 are also allowable at least by virtue of their dependence on allowable claims 1 and 7.

Reply to 35 U.S.C. 103 Rejection

The Examiner has rejected claims 5-6 and 12-13 under 35 U.S.C. 103 (a) as being unpatentable over Tsukahara as applied to claims 1 and 7 above and further in view of Applicants' Fig. 1 . Specifically the Examiner asserts that every element of the present invention is disclosed in Tsukahara with the exception of the incorporation of I-buttons. The Examiner goes on to assert that the I-buttons are disclosed in prior art Figs 1 and 2 thereby rendering the present invention obvious.

As traversed above with respect to the 35 U.S.C. 102 (b) rejections above, Tsukahara simply does not disclose the elements of the present invention and prior art figures 1 and 2 taken in combination with Tsukahara do not teach or suggest the apparatus disclosed in the present invention. Accordingly, Tsukahara does not render claims 5-6 and 12-13 of the present invention obvious. Moreover these claims are patentable at least by virtue of their dependence on patentable claims 1 and 7.

Request for Reconsideration pursuant to 37 CFR 1.111

Having responded to each and every ground for objection and rejection in the Office Action mailed on April 19, 2004, Applicant requests reconsideration in the instant application pursuant to 37 CFR 1.111 and requests that the Examiner allow claim(s) 1-13 and pass the application to issue. If there is any point requiring further attention prior to allowance, the Examiner is asked to contact Applicants' counsel who can be reached at the telephone number listed below.

Respectfully,

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